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Four-step Method for Growing High-quality GaAs Films on Si Substrate by Molecular Beam Epitaxy

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Abstract: To improve quality and repeatability of GaAs growth on Si substrate, a new method named as four-step growth was proposed by successively inserting a low temperature (LT) and a high temperature (HT) GaAs buffer layer between the GaAs nucleation layer and the normal GaAs epilayer. The grown layers through four-step method showed high quality, *i.e.* single domain structure, mirror-like surface even under strong white light, reduced surface roughness and less surface defects, as well as high repeatability. Even without any post-growth annealing process, a 1 μm thick GaAs epilayer with root mean square (RMS) roughness of only 2.1 nm in 5 μm× 5 μm scanning areas was obtained while the full width at half maximum (FWHM) value of the GaAs (004) peak from double crystal X-ray diffraction ω-scan was just 210.6 arcsec.

Key words: GaAs/Si; four-step growth; buffer layer; MBE (molecular beam epitaxy)

Compared with GaAs substrates, Si substrates have such advantages as larger size, lower cost, better mechanical strength, and higher thermal conductivity. In addition, due to the potential integration of well-developed Si integrated circuit technology with GaAs based optoelectronic devices, there has been a great deal of researches on heteroepitaxial growth of GaAs on Si substrates in order to obtain high quality GaAs films[1]. Up to now, several high quality GaAs films have been fabricated on Si by using a-GaAs/a-Si double-buffer layers[2], relaxed graded $Si_{1-x}Ge_x$ buffer layers[3-4], $SrTiO_3$ buffer layers[5] , and patterned Si substrates[6-7]. However, the most desirable approach is still to directly grow GaAs epilayers on Si with the merit that the heteroepitaxial growth could be easily performed in one growth run.

Associated with direct epitaxial growth of GaAs on Si substrate, three inherent issues exist, *i.e.* 4.1% lattice mismatch, 59% thermal expansion mismatch and anti-phase domains (APDs)[8]. The lattice mismatch will result in high-density threading dislocations propagating into the epilayers along with the growth process and the difference in the thermal expansion coefficients between GaAs and Si leads to stress resulting in microcracks when the substrate is cooled down[9]. Moreover, the APDs at the interfaces would also deteriorate the quality of the crystal[10]. In order to solve these problems, two-step growth method was proposed and became the most generally used technique to directly grow GaAs on Si substrate by either MBE or MOCVD. Concerned with this method, a low-temperature GaAs nucleation layer with small thickness[11-12] is grown at first, and then the second step is to grow normal GaAs epilayer at high temperature. In addition, misoriented Si (100) substrates[13] and post-growth annealing process[14] are frequently used so that APDs and the threading dislocations can be reduced further. Nevertheless, the reproducibility of this direct growth method is poor usually resulting in a milky GaAs/Si surface. And reports about the reasons and the improvements are scarce.

In this study, an improved growth technique named as four-step growth by inserting LT and HT GaAs buffers is proposed based on the two-step growth. Through this new approach GaAs/Si films with good morphology can be yielded repeatedly. Moreover, it is significantly positive to decrease defects and improve the quality of crystalline. And even without any post-growth thermal annealing process, GaAs thin films on Si with low values of RMS and FWHW are obtained. Meanwhile, two-step growth method has been investigated under optimized conditions while the reasons for frosted GaAs/Si surfaces and poor reproducibility are analyzed. Besides, the effects of LT and HT buffers in four-step growth have been also investigated.

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1 Experiment

A Riber 32P solid-source MBE system was employed to grow GaAs epilayers on Si (100) substrates. 3″ Phosphorus-doped Si (100) substrates with 4° misoriented towards the 〈110〉 planes were used in our experiments. The substrates were mounted on In-free Mo substrate holders after degreasing and drying process.

Oxide desorption was performed by holding the Si substrate at temperature about 800℃ for 5 min and then the substrate was thermally treated at 900℃ for 30 min in order to form sufficient double atomic steps for the suppression of APDs and part of dislocations[15]. Subsequently the substrate was cooled to 300℃ and exposed to As_2 for several minutes to form an As epilayer. Then, both two-step growth and four-step growth were carried out under optimized temperatures, Ⅴ/Ⅲ beam equivalent pressure (BEP) ratios and growth rates. For two-step growth, a 30 nm initial GaAs nucleation layer was grown at 300℃with a low growth rate of 0.1 μm/h, followed by 970 nm normal GaAs epilayer grown at 600℃ with a rate of 1.0 μm/h. And the Ⅴ/Ⅲ BEP ratios used for these two layers were 12 and 20, respectively. For four-step growth, based on two-step growth, a 100 nm-thick low temperature GaAs buffer layer was grown after the nucleation layer. The growth temperature, rate and Ⅴ/Ⅲ BEP ratio were 400℃, 0.1 μm/h and 14, respectively. Subsequently, a 100 nm-thick high temperature GaAs buffer layer was grown at 500℃ at a 0.3μm/h rate with a Ⅴ/Ⅲ BEP ratio value of 16. The schematic growth layer structures are illustrated in Fig. 1. In addition, the films grown without the LT GaAs buffer or the HT GaAs buffer were also studied in order to analyze the effects of the buffers in the four-step growth process.

Surface morphology of the GaAs/Si epilayers was characterized by scanning elctron microscope (SEM) and atomic force microscope (AFM). Crystalline perfection of GaAs epilayers was investigated by double crystal X-ray diffraction (DCXRD) ω scan. And the density of dislocations was evaluated through the FWHM value of the GaAs (004) diffraction peak, compared to the etch pit density (EPD) after etching with molten KOH at 300℃.

2 Results and discussion

2.1 Morphologies of GaAs films grown by the two methods

Firstly, 1 μm thick GaAs films were directly grown on Si substrates under optimized conditions by MBE through different methods. Fig. 2 shows the SEM micrographs of GaAs epilayers on Si by two-step growth and four-step growth. In Fig. 2(a), elongated pits are clearly observed and their major axis directions are all perpendicular to [011] azimuth of Si substrate indicating a single domain structure. In addition, a slightly wavy surfuce is also observed due to the possibility of large surface undulation. Conversely, a flat surface without large surface defects is obtained by four-step growth shown in Fig. 2(b).

The pits regarded as surface defects would degrade the quality of the GaAs films on Si substrate and they are considerd to be the main reason to cause milky surfaces. It is found that when the density of the elongated pits is lower than 10^7 cm^{-2} , the surface would look like a mirror under natural light but seem sligthly milky under strong light from LEDs. And when the density is higher than 10^7 cm^{-2}, a frosted surface will be seen even under natural light.

In previous researches[16-18], it has been shown that initial GaAs nucleation layer is started in a three-deminsional (3D) growth mode forming GaAs islands. As the thickness increases, 3D GaAs islands gradually coalesce to transform to a two-deminsional (2D) growth mode and a planar GaAs/Si surface is obtained at last. Under optimized growth conditions, small GaAs islands with high density and good uniformity that can easily coalesce would be formed. However, the 3D GaAs islands are unstable and can be easily rearranged or destroyed when heated at high growth temperature. So the elongated pits formed in two-step growth are thought to be the result of incomplete coalescence of GaAs islands which are partly rearranged or destroyed. In additon, GaAs islands rearranged or destroyed under high temperature are more random so that the reproducibility of two-step growth is poor. By introducing LT and HT GaAs buffer layers, it can not only protect the initial GaAs islands but also facilitate the coalescence process. As a result, a smooth GaAs epilayer surface without large defects is produced.

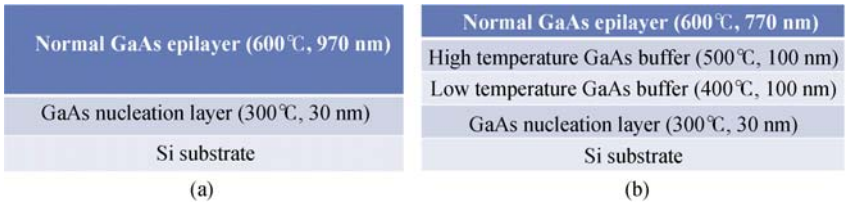

Fig. 1 The growth schemes of GaAs on Si for two-step growth (a) and four-step growth (b)

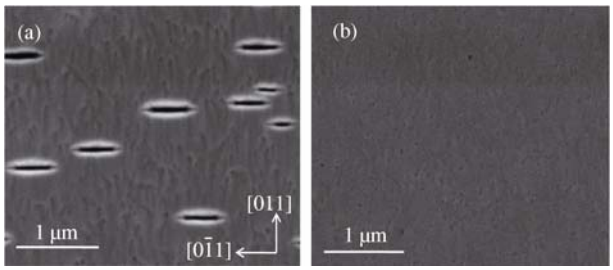

Fig. 2　SEM micrographs of GaAs epilayers on Si by two-step growth (a) and four-step growth (b)

In order to figure out the depth of the pits and the values of surface undulation, a cross-sectional profile was mesured by AFM along [011] azimuth of Si substrate acrossing several pits for the sample grown by two-step method. And another cross-sectional profile was also mesured along [011] azimuth for GaAs/Si surface grown by four-step method. The results are shown in Fig. 3.

As can be seen, the elongated pits formed in two-step growth have various depths from 15 nm to 51 nm indicating that they do not come directly from the substrate. And it is remarkable that the mean value of surface undulation (about 10 nm) even at the places where there is no pit is more than twice of that grown by four-step method. To our best knowledge, the lowest mean value is about 5.7 nm grown by MOVPE using a-GaAs/a-Si double-bufer layers[2] and there is no such low surface undulation reported as that produced by four-step growth through direct growth of GaAs epilayers on Si especially at 1 μm thickness.

Fig. 4 shows the etch pit morphologies of GaAs epilayers on Si. The GaAs epitaxial layers were all etched by molten KOH at 300℃ for about 3 s. The EPD is used to estimate the threading dislocation density in GaAs films on Si. As seen in Fig. 4, the EPD of GaAs epilayer by two-step growth is about 4.6×10^7 cm^{-2} while the EPD for four-step growth is about 6.9×10^6 cm^{-2}.

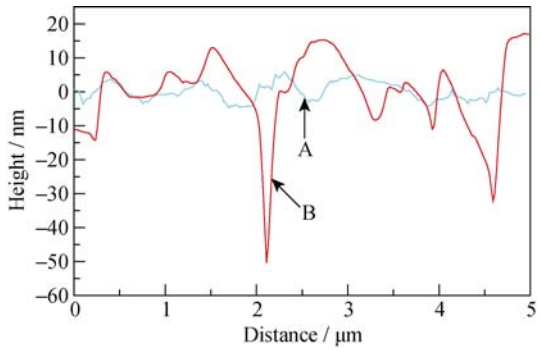

Fig. 3　Cross-sectional profile of GaAs epilayers on Si for four-step (A) and two-step growth (B)

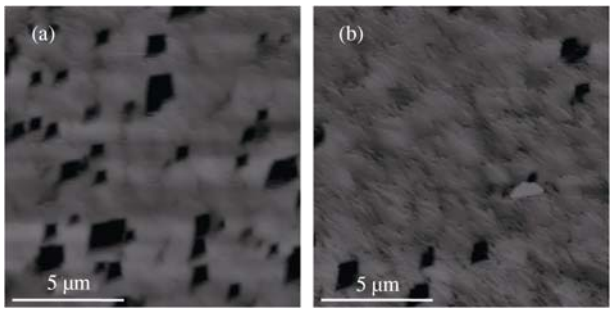

Fig. 4　Etch pit morphologies of GaAs epilayers on Si by two-step growth (a) and four-step growth (b)

It is well known that the threading dislocations in GaAs films are caused by the large lattice mismatch between GaAs and Si while the strained nucleation layer acts as an effective layer to reduce dislocations and restrict dislocations from moving. When the growth temperature is raised too high immediately after depositing the nucleating layer, most of the dislocations confined in the GaAs islands would glide and even penetrate into the surface. Through the striking contrast of the EPDs, it is concluded that the LT and HT GaAs buffer layers in four-step growth help to prevent the dislocations from penetrating into the GaAs epilayers to a large extent.

2.2　Roles of LT & HT buffers in four-step growth

In order to study the respective effect of each buffer layer in four-step growth, the AFM 3D morphologies of 200 nm GaAs epilayer grown on the nucleation layer at a 0.1 μm/h rate at different temperatures are investigated as shown in Fig. 5. Fig. 5(b) shows that when the 200 nm GaAs was grown at 500℃ after the completed nucleation layer, the prototypes of elongated pits marked with blue oval lines have already formed. But as seen in Fig. 5(a), the initial small and dense GaAs islands grow up and coalesce with no elongated pits when the growth temperature is 400℃. In addition, as long as the LT GaAs buffer layer is grown before growth at a relatively high temperature, the prototypes of elongated pits would not exist as shown in Fig. 5(c) and Fig. 5(d). Therefore, the LT GaAs buffer layer indeed plays an important role in promoting the coalescence process of GaAs islands and protecting the initial GaAs islands from being rearranged or even destroyed by high temperature. Through comparing the mean values of surface undulation shown in Fig. 5(a) (15.9 nm), Fig. 5(b) (12.9 nm) and Fig. 5(c) (10.1 nm), it is found that the HT GaAs buffer layer at 500℃ strengthens the radial growth of the GaAs islands and weakens the vertical growth indicating a further coalescence of GaAs islands and a beginning of formation of a planar surface. This is probably due to the enhanced migration of Ga atoms temperature is raised.

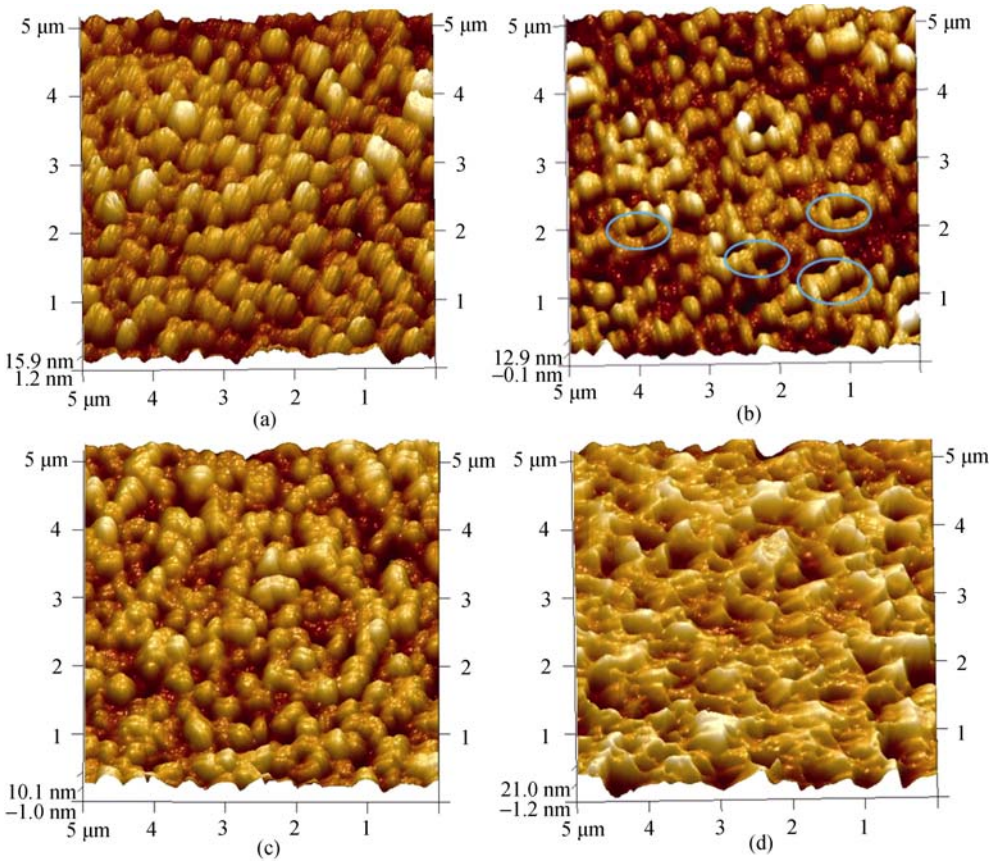

Fig. 5 AFM 3D images of 200 nm GaAs epilayer grown on the nucleation layer at different temperatures
(a) 400℃; (b) 500℃; (c) 400℃ (100 nm) + 500℃ (100 nm); (d) 400℃ (100 nm) + 600℃ (100 nm) over 5 μm × 5 μm scanning areas

However, if the temperature is raised further to 600℃ after the LT GaAs buffer layer, a wavy surface with a mean undulation value of 21.0 nm is obtained, as shown in Fig. 5(d). It is concluded that raising the growth temperature too high before complete coalescence of initial GaAs islands would result in a relatively rough GaAs/Si surface because of much more release of the remaining stress in GaAs islands in the form of surface undulation.

As the thickness of GaAs epilayer increases, the initial 3D growth mode gradually transforms to 2D growth mode. But the surface undulation and the density of surface defects would vary with different growth process. As shown in Fig. 6(a) and 6(c), elongated pits formed at early stage have shaped up on the surface without the LT GaAs buffer. In three-step growth without the HT GaAs buffer, a wavy surface without elongated pits is formed as seen in Fig. 6(b). So in order to obtain a good morphological GaAs/Si surface as shown in Fig. 6(d), the LT and HT GaAs buffer layers are all necessary, considering that the initial GaAs islands in the nucleation layer need to be protected and merge sufficiently before growing normal GaAs epilayers. RMS roughness values of films shown in Fig. 6(a), 6(b), 6(c) and 6(d) are 4.9 nm, 3.2 nm, 4.2 nm and 2.1 nm in a 5 μm×5 μm scanning area,

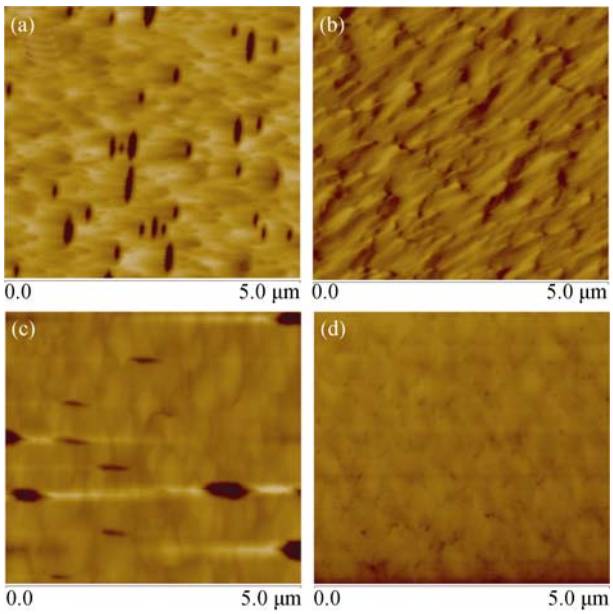

Fig. 6 AFM images of 1-μm-thick GaAs epilayers grown on Si with different growth process in a 5 μm×5 μm scanning area
(a) Two-step growth; (b) Three-step growth without high temperature GaAs buffer; (c) Three-step growth without low temperature GaAs buffer; (d) Four-step growth

respectively. Up to now, the lowest RMS roughness value ever reported is about 1.5 nm in a 2 μm×2 μm scanning area for a 3 μm-thick GaAs on Si without thermal

annealing grown by MBE[12]. In our experiments, the measured value for the sample grown by four-step growth over 2 μm×2 μm scanning area is 1.8 nm. But it is believed that the value would decrease further as the increase of thickness.

Fig. 7 shows GaAs (004) ω-scan measured by DCXRD for 1 μm-thick GaAs epilayers on Si with different processes. It is obvious that the film grown by four-step growth has the smallest FWHM value of 210.6 arcsec which is the best value ever reported for samples of such thickness without thermal annealing, corresponding to a crystal of good quality. The FWHM value for two-step growth is 397.9 arcsec and decreases to 311.3 arcsec and 376.6 arcsec by inserting the LT buffer and HT buffer, respectively, which explains that the low temperature buffer and high temperarure buffer help to improve the crystal quality of GaAs on Si signally. It is well known that the FWHM value of DCXRD peak can be used to estimate the dislocation density of the epitaxial films according to the formula[19] as follows:

$$D = (\mathrm{FWHM})^2/4.36\boldsymbol{b}^2,\ \boldsymbol{b} = \frac{1}{2}a\langle 004\rangle$$

Where D is the density of dislocations, FWHM is expressed in rad, $\boldsymbol{b}$ is the dislocations Burgers vector and a is the lattice constant of GaAs. As calculated from this formula, the dislocation density for four-step growth is1.9×10^7 cm^{-2} while the value for two-step growth is 7.1×10^7 cm^{-2}. The dislocation density calculated by the FWHM value is higher than the EPD value discussed above. The reason for this is that two or more threading dislocations may join together to form one big etch pit, and not all dislocations are revealed as etch pits.

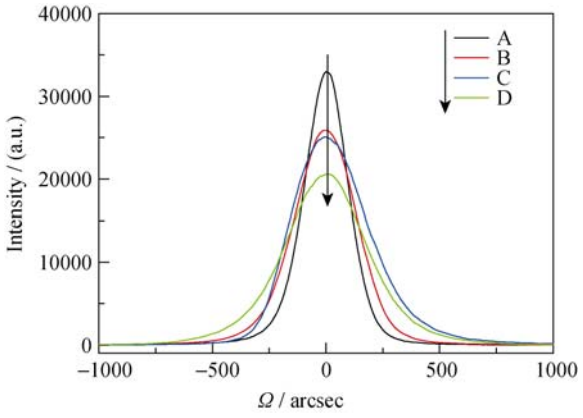

Fig. 7　GaAs (004) ω-scan measured by DCXRD for 1 μm-thick GaAs epilayers on Si with different process
(A) Four-step growth; (B) Three-step growth without HT GaAs buffer; (C) Three-step growth without LT GaAs buffer; (D) Two-step growth

3. Conclusion

We have proposed a four-step growth method to produce high-quality GaAs films on Si substrates. Compared with the conventional two-step growth, the reproducibility is improved to a large extent while it can dramatically decrease the threading dislocations, improve the surface morphology and crystalline quality of GaAs layers on Si. And a 1 μm thick GaAs epilayer with RMS roughness of only 2.1 nm was obtained by four-step growth. Threading dislocation density is 1.9×10^7 cm^{-2} calculated from XRD FWHM value and the EPD is about 6.9×10^6 cm^{-2}. It is concluded that the low temperature and high temperature GaAs buffer layers can effectively protect the unstable nucleation layer and promote the coalescence process of initial GaAs islands. Consequently, a mirror-like GaAs epilayer surface with less surface defects and dislocations could be produced steadily compared with two-step growth. It is believed that the high-quality GaAs epilayers grown on Si substrates through this new method could lay a good foundation on realizing monolithically integrated Ⅲ-Ⅴ optoelectronic devices on Si.

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四步法制备高质量硅基砷化镓薄膜

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摘 要: 为了提高在硅基上外延砷化镓薄膜的质量和实验的可重复性, 我们提出了一种叫做四步生长法的新方法, 该方法是通过在低温成核层和高温外延层中间先后插入低温缓冲层和高温缓冲层实现的。通过此方法, 可以制备出表面具有单畴结构、在强白光下依然光亮如镜、粗糙度低且缺陷少的高质量砷化镓薄膜, 而且此方法的重复性很好。即便没有任何生长后的退火处理, 外延出的 1 μm 厚砷化镓薄膜在 5 μm×5 μm 扫描区域内的表面粗糙度只有 2.1 nm, 且由 X 射线双晶衍射测试出的砷化镓(004)峰的半高宽只有 210.6 arcsec。

关 键 词: 硅基砷化镓; 四步生长法; 缓冲层; 分子束外延

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